WHAT IS CLAIMED IS:

1. A processor comprising:

a prediction circuit configured to predict an execution latency of a floating point operation; and

a floating point unit coupled to receive the floating point operation for execution, wherein the floating point unit is configured to detect a misprediction of the execution latency.

2. The processor as recited in claim 1 wherein the prediction circuit is configured to predict the execution latency responsive to a predicted precision of operands of the floating point operation.

3. The processor as recited in claim 2 wherein the floating point unit comprises a control register storing a precision control indication indicative of an output precision for floating point operation, wherein the predicted precision is the output precision.

4. The processor as recited in claim 2 wherein the floating point operation is a multiply operation, and wherein the floating point unit comprises a multiplier designed for a first precision less than a maximum precision supported by the processor, and wherein the execution latency is based on a number of passes through the multiplier used to complete a multiplication of the precision of the operands.

5. The processor as recited in claim 2 wherein the floating point unit comprises a precision check circuit coupled to receive the operands of the floating point operation, wherein the precision check circuit is configured to detect the misprediction if at least one of the operands of the floating point operation has a precision that exceeds the predicted

precision.

6. The processor as recited in claim 1 further comprising a scheduler coupled to the floating point unit, wherein the scheduler is configured to schedule the floating point operation for execution by the floating point unit, and wherein the floating point unit is configured to signal the scheduler responsive to detecting the misprediction.

7. The processor as recited in claim 6 wherein the scheduler is configured to reschedule the floating point operation responsive to the signaling from the floating point unit with the execution latency indicated as a latency detected by the floating point unit.

8. The processor as recited in claim 6 wherein the prediction circuit is configured to predict the execution latency of the floating point operation responsive to dispatch of the floating point operation to the scheduler.

9. The processor as recited in claim 6 further comprising a trace cache configured to store predicted operation traces, wherein the prediction circuit is configured to predict the execution latency responsive to the floating point operation being included in a trace, and wherein the trace cache is configured to store an indication of the execution latency predicted by the prediction circuit.

10. The processor as recited in claim 9 wherein the trace cache is configured to store a selected opcode of at least two opcodes for the floating point operation responsive to the execution latency predicted by the prediction circuit, the selected opcode comprising the indication of the execution latency.

11. The processor as recited in claim 1 wherein the floating point unit is configured to signal an exception responsive to detecting the misprediction.

12. The processor as recited in claim 11 wherein the processor is configured to refetch the floating point operation responsive to the exception.

13. The processor as recited in claim 1 wherein the floating point unit is configured to detect the misprediction responsive to detecting an actual execution latency greater than the execution latency predicted by the prediction circuit.

14. The processor as recited in claim 13 wherein the floating point unit is configured not to detect the misprediction responsive to detecting the actual execution latency is less than the execution latency predicted by the prediction circuit.

15. The processor as recited in claim 13 wherein the floating point unit is further configured to detect the misprediction responsive to detecting the actual execution latency is less than the execution latency predicted by the prediction circuit.

16. A method comprising:

predicting an execution latency of a floating point operation;

scheduling the floating point operation for execution in a floating point unit; and

the floating point unit detecting a misprediction of the execution latency.

17. The method as recited in claim 16 wherein the predicting is responsive to a predicted precision of operands of the floating point operation.

18. The method as recited in claim 17 wherein the floating point operation is a multiply operation, and wherein the floating point unit comprises a multiplier designed for a first precision less than a maximum precision supported by the processor, and wherein the

execution latency is based on a number of passes through the multiplier used to complete a multiplication of the precision of the operands.

19. The method as recited in claim 17 wherein detecting the misprediction comprises detecting that at least one of the operands of the floating point operation has a precision that exceeds the predicted precision.

20. The method as recited in claim 16 further comprising rescheduling the floating point operation responsive to detecting the misprediction, with the execution latency indicated as a latency detected by the floating point unit.

21. The method as recited in claim 16 further comprising:

signaling an exception responsive to detecting the misprediction; and

refetching the floating point operation responsive to the exception.

22. The method as recited in claim 16 wherein detecting the misprediction comprises detecting an actual execution latency greater than the execution latency predicted in the predicting.

23. The method as recited in claim 22 further comprising not detecting the misprediction responsive to detecting the actual execution latency is less than the execution latency predicted in the predicting.

24. The method as recited in claim 22 further comprising detecting the misprediction responsive to detecting the actual execution latency is less than the execution latency predicted in the predicting.